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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,295	08/31/2000	Allen Yen	3-6-16	4287

7590 08/04/2003

Docket Administrator (Room 3C-512)
Lucent Technologies Inc
600 Mountain Avenue P O Box 636
Murray Hill, NJ 07974-0636

EXAMINER	
NGUYEN, CUONG QUANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/653,295	Applicant(s) YEN ET AL.	
	Examiner Cuong Q Nguyen	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *7-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The finality in paper number 10 filed on 8-26-01 has been withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saia et al. (US 5,736,448 in view of Watanabe et al. (US 5,481,490) and further in view of Kendall et al. (US 3,962,713).

Regarding claims 1-3, Saia et al. discloses an integrated circuit (col.2 lines 24-27) comprising: a first interconnect level (the level of a conductive layer 20); a second interconnect level (the level of a conductive layer 52); a third interconnect level (the level of a conductive layer 58 on an insulating layer 56); a stack of alternating conductive and insulative layers formed in vertical alignment with respect to an underlying plane, wherein the stack layers formed between the first and second interconnect levels and including a first conductive layer (36), a first insulator layer (38) on the first conductive layer, a second conductive layer (40) on the first insulative layer, a second insulative layer (42) on the second conductive layer, and a third conductive layer (44) on the second insulative layer with the first and third conductive layer

commonly connected through the first , second and third interconnect levels. See Saia et al.'s Fig.7-9.

Saia et al. does not explicitly teach that the integrated circuit is a monolithic integrated circuit and the first and second interconnect levels to semiconductor layer.

It is well known in the art and also taught by Watanabe et al. that the capacitor structure is commonly connected to a semiconductor layer such as source/drain region of the FET transistor in order to control the charge storage in the capacitor structure by ON/OFF states of the FET transistor.

It is conventional and also taught by Kendall et al. teaches that the capacitor structure can be formed in a discrete semiconductor device or in a monolithic integrated circuit. Saee Kendall et al.'s col.8 lines 54-60.

Therefore, it would have ben obvious to one of ordinary skill in the art connecting the first and second interconnect levels to semiconductor layer in Saia et al.'s device and the capacitor is formed in a monolithic integrated circuit as taught by Kendall et al.

Regarding claim 5, as shown in Saia et al.'s Fig.7-9, the level of layer (58) on the insulating layer (56) is considered as the second interconnect level and the stack of alternating conductive and insulative layers between the first interconnect level (the level of layer 20) and the second interconnect level includes one more pair of addition conductive and insulative layers (a third insulative layer 46, a fourth conductive layer 48, a fourth insulative layer 50, a fifth conductive layer 52) formed over the third conductive

layer providing the uppermost layer (52) commonly connected with the first and third conductive layers.

Regarding claim 6, it is noted that the Saia et al.'s device is identical as claimed structure such that the fifth conductive layer (52) commonly connected with the first conductive layer (36) and third conductive layer (44). Therefore, it is inherent that Saia et al.'s device comprises 5 conductive layers configured to provide 4 capacitors connected in parallel.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saia et al. in view of Watanabe et al., Kendall et al. and further in view of Roy (US 6,180,976).

Saia et al., Watanabe et al. and Kendall et al. teach all the limitations of claims 1-3 and 5-6 as shown above and further teaches that the first interconnect level including a via portion and a trench portions. Saia et al. and Watanabe et al. do not teach that the interconnect levels including a trench portions of a Damascene structure.

Roy discloses a capacitor structure comprises a multi-level of interconnections connected to a capacitor structure and the multilevel of interconnection can be formed of a single or dual damascene interconnection structure. See Roy's Fig.10, Fig.13 and col.4 lines 1-7.

Roy clearly established that it is conventional to form the interconnection by a single or dual damascene interconnection structure. Therefore, it would have been obvious to one of ordinary skill in the art to form the interconnect levels of the device

formed by the combination of Saia et al., Watanabe et al. and Kendall et al. of damascene structure.

Response to Arguments

3. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the

TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

6. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

Primary examiner

July 29, 2003